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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/764,150	01/23/2004	Dennis E. Dudeck	1-4-32-5	8145

7590 12/05/2005

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EXAMINER	
NGUYEN, TAN	
ART UNIT	**PAPER NUMBER**
2827	

DATE MAILED: 12/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/764,150	DUDECK ET AL.	
	Examiner	Art Unit	
	Tan T. Nguyen	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *16-21* is/are allowed.

6)☒ Claim(s) *1-15 and 22-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The amendment submitted by Applicants on November 17, 2005 has been received and entered.

2. Claims 1-26 are pending.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3, 6-8, 11-13 and 22-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Troutman (U.S. Patent No. 3,848,236) or Fournel et al. (U.S. Patent No. 6,307,797).

Regarding claims 1, 6, 11 and 22, Troutman disclosed in Figure 1 a read only memory [11] (column 3, line 9) comprises a plurality of transistors [28, 29, 30, 31] (column 4, lines 8-11) (which are called address field effect transistors), a threshold circuit [13] (column 3, line 10-12) receiving information read out of the memory. Troutman disclosed in Figure 2 a read operation of the ROM [11], a plurality of precharge transistors [21-26] are turned on during the precharge interval by the [Φ_{1+2}] clock signal to precharge columns [15-20] to a true voltage level. Thereafter, during the evaluation interval, depending in the presence or absence of the address field effect transistors [28-31], the column [15-20] is conditionally discharged to a false or true level (column 4, lines 30-56).

Troutman disclosed the operating cycle of the system is controlled by the two clock signals, which are conventionally available in prior four-phase logic systems. The

[Φ_{1+2}] clock signal has a logic one or true level during first and second phase time intervals viz. Φ_1 and Φ_2 and has zero or false level at all other times. The [Φ_{3+4}] clock signal has a logic one or true level during third and fourth time intervals viz. Φ_3 and Φ_4 and zero or false level otherwise. Troutman further disclosed the true intervals of the two clock signals are separated by in-between time intervals designated [IB], and the true interval of the [Φ_{1+2}] clock signal will be preferred to as the first or precharge interval, while the true interval of [Φ_{3+4}] clock signal will be preferred as the second or evaluation interval (column 3, lines 18-30). Accordingly, Trouman clearly showed in Figure 2 the precharge interval is positioned prior to the evaluation interval for the read cycle.

Regarding claims 2, 7, 12 and 23, Troutman showed in Figure 2 that the precharge interval is terminated by the rising edge of the clock signal [Φ_{1+2}].

Regarding claims 3, 8, 13 and 24, Troutman showed in Figure 2 that the precharge interval lasts for approximately one-half of the read operation.
Fournel disclosed in Figure3 a read cycle having a precharging phase positioned prior to an evaluation phase (column 7, lines 32-33). Fournel further disclosed in Figure 1 the memory device having current/voltage converters [C_{IVD}] and [C_{IVR}] which precharge the bit lie [BL] and [BL_{REF}] to a precharging voltage [Vbias1] in the precharging phase(column 6, lines 16-37, column 8, lines 55-57). Fournel disclosed in the following phase of evaluation, the precharging circuits are stopped and the read current generator is activated (column 7, lines 45-46).

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 4-5, 9-10, 14-15 and 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Troutman in view of Mashiko et al. (U.S Patent No. 4,833,653).

See description of Troutman in paragraph 4, supra. Troutman did not discuss the precharge phase is internal timed out prior to a subsequent clock edge.

Regarding claims 4, 9, 14 and 25, Mashiko et al. disclosed in Figures 1-3 a memory device wherein when the external clock signal Ext.RAS falls, the internal signal [/RAS] also falls in response to the external clock signal Ext.RAS, then the equalizing transistors [13A,13B,23A,23B] are turned off. As a result, precharging of the bit lines is completed (column 4, lines 12-24).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the memory device of Troutman by providing the internal signal of Mashiko et al.

The rationale is as follows: A person of ordinary skill in the art would have been motivated to use the internal signal of Mashiko et al. to end the precharge cycle independently from the external clock signal.

Regarding claims 5, 10, 15 and 26, Troutman showed in Figure 2 the precharge interval is less than one-half of the read cycle.

7. <u>REMARKS</u>

Regarding independent claims 1, 6, 11 and 22, Applicants amended the claims so that require a precharge phase prior to an evaluation phase for **each** read cycle. Applicants asserted in the REMARKS that Troutman does not disclose or suggest requiring a precharge phase prior to an evaluation phase for **each** read cycle. The Examiner disagreed with Applicants' argument. What Troutman showed in figure 2 is an operating cycle, which is a read cycle, this read cycle is conventionally performed every time a read operation is activated. The read cycle is controlled by the two clock signals which are conventionally available in prior four-phase logic systems. Troutman showed in Figure 2 the two clock signals [Φ_{1+2}] and [Φ_{3+4}] separately, however, if these two clock signals are superimposed on top of the other then it is clear that the [Φ_{1+2}] clock signal has a logic one or true level during first and second phase time intervals viz. Φ_1 and Φ_2 and has zero or false level at all other times. The [Φ_{3+4}] clock signal has a logic one or true level during third and fourth time intervals viz. Φ_3 and Φ_4 and zero or false level otherwise. The true intervals of the two clock signals are separated by in-between time intervals designated [IB], and the true interval of the [Φ_{1+2}] clock signal will be preferred to as the first or precharge interval, while the true interval of [Φ_{3+4}] clock signal will be preferred as the second or evaluation interval (column 3, lines 18-30). Accordingly, Troutman clearly showed in Figure 2 the precharge interval is positioned prior to the evaluation interval for the read cycle.

Applicants further asserted that "the leakage problem of the present application was not an issue in 1973 at the time Troutman was filed. Thus Troutman cannot be said to disclose or suggest a method for reducing leakage current". Although Troutman

did not discuss the issue of leakage current, but Troutman disclosed a read cycle having a precharge interval prior to an evaluation interval, which is similar to the method claimed by Applicant. Accordingly, the read cycle disclosed by Troutman would achieve the same result as the method claimed by Applicants.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Pascucci is cited to show a memory device having read cycle including precharge and evaluation phases.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tan T. Nguyen whose telephone number is (571) 272-1789. The examiner can normally be reached on Monday to Friday from 07:00 AM to 03:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian, can be reached at (571) 27201852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tan T. Nguyen
Primary Examiner
Art Unit 2827
November 30, 2005